APPENDIX A

"CLEAN" VERSION OF EACH PARAGRAPH/SECTION/CLAIM
37 C.F.R. § 1.121(b)(ii) AND (c)(i)

SPECIFICATION:

Attached is a replacement page for page 1 of the application.

CLAIMS (with indication of amended or new):

Please amend claim 1 as follows:

B1

1. (Amended) A current sense integrated circuit, comprising:

an amplifier circuit for receiving and amplifying a differential analog input signal at a first voltage level containing current sense information, wherein the amplifier circuit includes a circuit to minimize inherent temperature offset drift;

a pulse width modulator circuit for converting the differential analog input signal to a pulse width modulated signal at the first voltage level;

a level shift circuit for converting the pulse width modulated signal from the first voltage level to a second voltage level; and

a recovery circuit for reconstructing the analog input signal at the second voltage level.

B2

2 ~~3~~. (Amended) The current sense integrated circuit of claim 1, wherein the circuit to minimize inherent temperature offset drift comprises a pair of mirrored MOSFETs, such that the circuit has an offset voltage which is equal to the difference between the gate-to-source voltage of the MOSFETs and remains constant over temperature variations.

B3

3 ~~5~~. (Amended) The current sense integrated circuit of claim 1, wherein the level shift circuit comprises a pulse generator circuit for producing rising edge triggered pulses and falling edge triggered pulses from the pulse width modulated signal and a pair of MOSFETs for receiving the rising edge triggered pulses and the falling edge triggered pulses and transposing those pulses from the first voltage level to the second voltage level.

B3 concld

4 6. (New) The current sense integrated circuit of claim 1, further comprising a high side current reference circuit.